

Application No.: 10/718,455

Docket No.: JCLA12114

In The Specification:

Please amend the title of the present application to "PACKAGE PROCESS".

Please amend the following paragraphs:

[0001] The present invention relates to a ~~frame-attaching~~ package process, and more particularly to a process of attaching a transparent substrate to a chip using a frame sealant under a negative pressure for reducing the possibility of frame sealant from cracking.

[0004] Generally, an active area of an optical-electronic chip has a functional area serving for sensing, illuminating or other functions. In order to protect the functional area, a transparent substrate, such as a glass substrate, is attached to the functional area of active area of the chip using a frame sealant. The functional area of active area of the chip is covered by the transparent substrate and the frame sealant; therefore, a sealed space is formed and prevents moistures and particles from the sealed space.

[0006] As shown in FIG. 1B, a frame sealant 130 is formed on the active area 122 of the CIS chip 120, and the frame sealant 130 surrounds the sensing area 122a. As shown in FIG. 1C, the attaching surface 112 of the glass substrate 110 is attached to the frame sealant formed on the active area 122 of the chip 120.

[0007] Referring to FIGS. 1C and 2, FIG. 2 is the top view showing the CIS chip after package. In order to clarify the issue of frame sealant cracking, the glass substrate 110 is not shown in FIG. 2. It should be noted that the sealed space is formed and a pressure therein is increased because of the attaching process for glass substrate 110 and CIS chip 120. However, when the pressure difference between inside and outside of the sealed space is so large that the frame sealant 130 is easy to crack.

Application No.: 10/718,455

Docket No.:JCLA12114

[0008] The conventional ~~frame-attaching package~~ process is performed under atmosphere to attach the glass substrate to the chip. Because of the pressure difference between inside and outside of the sealed space, the phenomenon of frame sealant cracking easily occurs. Therefore, a sealed space cannot be formed on the active area of the optical-electronic chip, and moistures and particles enter into the sealed space and adversely affect the normal operation of the chip.

[0009] Therefore, one object of the present invention is to provide a ~~frame-attaching package~~ process for reducing the possibility of frame sealant cracking when the transparent substrate is attached to the chip and thereby increase the yield.

[0010] In accordance with the object of the present invention described above, the present invention provides a frame sealant attaching process adapted to attach an attaching surface of a transparent substrate to an active area of a chip using a frame sealant, wherein the active area of the chip further comprises a functional area. The frame sealant attaching process comprises: forming the frame sealant on the active area of the chip, wherein the frame sealant surrounds the functional area; attaching the attaching surface of the transparent substrate to the frame sealant formed on the active area of the chip under a negative pressure; and solidifying the frame sealant.

[0011] The present invention further provides a ~~frame-attaching package~~ process adapted to attach an attaching surface of a transparent substrate to an active area of a chip using a frame sealant, wherein the active area of the chip further comprising a functional area. The frame sealant attaching process comprises: forming a frame sealant on the attaching surface of the transparent substrate; attaching the frame sealant formed on the attaching surface of the

Application No.: 10/718,455

Docket No.:JCLA12114

transparent substrate to the active area of the chip under a negative pressure, the frame sealant surrounding the functional area; and solidifying the frame sealant.

[0012] According to the ~~frame-attaching package~~ process of the present invention, the negative pressure is from about 0.5 to about 0.9 atmospheres. In addition, the method of solidifying the frame sealant is accomplished by exposing the frame sealant to an ultraviolet light.

[0013] According to the present invention, a frame sealant may be formed on the attaching surface of the substrate or the active area of the chip and then attach the attaching surface of the substrate to the active area of the chip using the frame sealant under a negative pressure. Because the pressure difference between the inside and outside of the frame sealant is reduced, the possibility of frame sealant cracking is reduced and the yield of ~~frame-attaching package~~ process is improved.

[0017] FIGS. 3A-3D are schematic views illustrating the progression of steps of a first exemplary ~~frame-attaching package~~ process in accordance with the present invention.

[0018] FIGS. 4A-4D are schematic views illustrating the progression of steps of a second exemplary ~~frame-attaching package~~ process in accordance with the present invention.

[0020] Please referring to FIGS. 3A-3D, they are a schematic process flow showing a first exemplary ~~frame-attaching package~~ process in accordance with the present invention.

[0022] As shown in FIG. 3B, a frame sealant 330 is formed on the active area 322 of the chip 320, and the frame sealant 330 surrounds the functional area 322a.

[0023] As shown in FIG. 3C, a negative pressure is provided, which ranges from about 0.5 to about 0.9 atmospheres. The negative pressure is generated from, for example, a vacuum system. The vacuum system includes a chamber 342, a vacuum pump 344, a valve 346 and a

Application No.: 10/718,455

Docket No.: JCLA12114

pressure meter 348. The vacuum pump 344 serves to generate the negative pressure from about 0.5 to about 0.9 atmospheres. Moreover, the transparent substrate 310 and the chip 320 are moved in the chamber 342 and the attaching surface 312 of the transparent substrate 310 is attached to the frame sealant 330 formed on the active area 322 of the chip 320 under the negative pressure.

[0024] As shown in FIG. 3D, the frame sealant 330 is solidified, wherein the method of solidifying the frame sealant is accomplished by exposing the frame sealant 330 to an ultraviolet light or by using some other methods.

[0025] In addition to the first ~~frame-attaching~~ package process, the present invention discloses a second ~~frame-attaching~~ package process in which the difference between the first and second processes is that instead of forming the frame sealant on the chip as described in the first ~~frame-attaching~~ package process, the frame sealant is formed on the transparent substrate for attaching to the chip.

[0026] Referring to FIGS. 4A-4D, are a schematic views illustrating a second exemplary ~~frame-attaching~~ package process in accordance with the present invention.

[0027] As shown in FIG. 4A, a transparent substrate 310 and a chip 320 are provided. The descriptions of transparent substrate 310 and the chip 320 are the same described in the first ~~frame-attaching~~ package process and therefore is not repeated herein.

[0028] As shown in FIG. 4B, a frame sealant 330 is formed on the attaching surface 312 of the transparent substrate 310 and corresponds to the perimeter of the active area 322 of the chip 320.

Application No.: 10/718,455

Docket No.: JCLA12114

[0029] As shown in FIG. 4C, the transparent substrate 310 and the chip 320 are moved in the vacuum system 340, wherein the vacuum pump 344 serves to generate the negative pressure from about 0.5 to about 0.9 atmosphere in the chamber 342. Moreover, the transparent substrate 310 and the chip 320 are moved in the chamber 342 and the frame sealant formed on the attaching surface 312 of the transparent substrate 310 is attached to the active area 322 of the chip 320.

[0030] As shown in FIG. 4D, the frame sealant 330 is solidified, wherein the method of solidifying the frame sealant is accomplished by exposing the frame sealant 330 to an ultraviolet light or by using some other methods.

[0031] Referring to FIGS. 3D, 4D and 5, FIG. 5 is a top view showing the package structure of FIGS. 3D and 4D. In order to describe the position of the frame sealant 330, the transparent substrate 310 shown in FIGS. 3D and 4D is not shown. It should be noted that although a higher pressure exists within a sealed space formed by the transparent substrate 310, the chip 320 and the frame sealant 330 than outside of the chamber caused by attaching the transparent substrate 310 the chip 320, the frame sealant cracking could barely occur because the chamber pressure was maintained in a negative pressure ranging between about 0.5 to about 0.9 atmosphere during the ~~frame-attaching~~ package process.

[0032] From the descriptions mentioned above, in the ~~frame-attaching~~ package process, the attaching surface of the transparent substrate is attached to the frame sealant formed on the active area of the chip under a negative pressure and that the frame sealant surrounds the functional area. It is to be noted that the frame sealant can be formed on either on the attaching surface of the transparent substrate or on the active area of the chip. In the ~~frame-attaching~~

Application No.: 10/718,455**Docket No.:JCLA12114**

package process of the present invention, because the pressure within the sealed space where the transparent substrate, the chip and the frame sealant are attached is low, and therefore the pressure difference between the inside and outside of the sealed frame sealant is reduced. Therefore, the possibility of frame sealant cracking is reduced and the yield of ~~frame-attaching~~ package process is improved.

[0033] In addition, the ~~frame-attaching~~ package process of the present invention can be applied to Charge-Coupled Device (CCD), CMOS Image Sensor (CIS), solar cells, Bio-chips and the other optical-electronic devices, so that the possibility of frame sealant cracking thereof can be effectively reduced and thereby improve the yield of ~~frame-attaching~~ package process.